wherein the alternating conductivity type layer comprises first semiconductor regions of a firstconductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged in a surface portion of the major surface; and

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes .

2 (Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged; and

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes;

wherein the alternating conductivity type layer comprises first sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch, and second sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch different from the first pitch.

~~6. (Amended) A lateral semiconductor device comprising:~~

~~a semiconductor chip;~~

~~two main electrodes on one major surface of the semiconductor chip; and~~

~~an alternating conductivity type layer between the main electrodes;~~

~~wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;~~

~~wherein the first semiconductor regions and the second semiconductor regions are alternately arranged;~~

~~wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes;~~

~~wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section; and~~

~~wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at the first pitch in the straight sections, and the first semiconductor regions and the second semiconductor regions are arranged alternately at the second pitch in the curved sections.~~

REMARKS

The Examiner has indicated claims 2, 6 and 7 would be allowable if rewritten in independent form. Applicants have rewritten claims 2 and 6 as independent claims, thereby placing the claims in condition for allowance. Claim 7 depends on claim 6 and should there also be in condition for allowance. Further, applicants request rejoinder of claims 7-12, which depend either directly or indirectly on claim 6, as claim 6 is now indicated as allowable and a generic linking claims to claims 7-12. Claims 2 and 6-12 are therefore in condition for allowance.